AUG 07 2006

PATENT

reby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Alexandra Beggs

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Kang Yong Kim and Gary

Attorney Docket No.: 501313.01

Johnson

Patent No. : US 6,812,760 B1

Serial No.

: 10/613,302

Issue Date: November 2, 2004

Filed

: July 2, 2003

Title

: SYSTEM AND METHOD FOR COMPARISON AND COMPENSATION OF FINE

DELAY VARIATIONS BETWEEN FINE DELAY AND COARSE DELAY

**CIRCUITS** 

## REQUEST FOR CERTIFICATE OF CORRECTION

Certificate

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 AUG 1:0 2006

of Correction

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line

Reads

Should Read

Column 1, Line 49

"the phase-shift"

-- the phase shift--

Column 3, Line 17

"VD as a value"

-- VD has a value--

Column 3, Line 29

"phase detector 10"

-- phase detector 110--

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Column 3, Line 60	"each cycle of the"	at each cycle of the
Column 3, Line 64	"until the delaylocked"	until the delay locked
Column 6, Line 11	"schematic drawing the"	schematic drawing of the
Column 7, Line 21	"signal, erratic, and non- linear"	signal, erratic and non-linear
Column 7, Line 60	"if rippling present"	if rippling is present
Column 8, Line 61	"appreciated, that"	appreciated that
Column 9, Line 45	"embodiment the fine/coarse"	embodiment of the fine/coarse
Column 10, Line 12	"fine delay. circuit"	fine delay circuit
Column 10, Line 54	"shift register having"	shift register having a
Column 11, Line 59	"thus, causing"	thus causing
Column 12, Line 2	"the SHIF d"	the SHIFTd
Column 13, Line 47	"32 bits words"	32 bit words
Column 13, Line 63	"received N/2 bits"	received N/2 bit
Column 15, Line 18	"such as output"	such output
Column 22, Line 18	"by reference"	by a reference

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original applications. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: // 2006

By: \_

Edward W. Bulchis, Reg. No. 26,847

Customer No. 27,076
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101

(206) 903-8785 Attorney for Applicant(s)

EWB:tdp

**Enclosures:** 

Postcard

Form PTO-1050 (+ copy)

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## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.

US 6,812,760 B1

DATED

November 2, 2004

INVENTOR(S)

Kang Yong Kim and Gary Johnson

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

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MAILING ADDRESS OF SENDER:

DORSEY & WHITNEY LLP 1420 Fifth Avenue, Suite 3400 Seattle, Washington 98101 Patent No. <u>US 6,812,760 B1</u>

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**→** 

FORM PTO-1050 (REV. 3-82)

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